| PART A: Introduction | | | | |
|---|---|---|---|---|
| Program: **Certificate** | | Class: **B.Sc.** | Year: **I Year** | Session: **2021-22** |
| Subject: **Computer Science** | | | | |
| 1. | Course Code | **S1-COSC 1T** | | |
| 2. | Course Title | **Computer System Architecture ( Paper 1 )** | | |
| 3. | Course Type (Core Course/Elective/Generic Elective/ Vocational | **Core Course** | | |
| 4. | Pre-Requisite (if any) | To study this course, a student must have had the subject Physics/Maths in 12th class. | | |
| 5. | Course Learning Outcomes(CLO) | **On completion of this course, learners will be able to:**<br>1. Understand the basic structure, operation and characteristics of digital computer.<br>2. Be able to design simple combinational digital circuits based on given parameters.<br>3. Familiarity with working of arithmetic and logic unit as well as the concept of pipelining.<br>4. Know about hierarchical memory system including cache memories and virtual memory.<br>5. Understand concept and advantages of parallelism, threading, multiprocessors and multicore processors.<br>6. Know the contributions of Indians in the field of computer architecture and related technologies. | | |
| 6. | Credit Value | **Theory – 4 Credits** | | |
| 7. | Total Marks | Max. Marks : **25+75** | | Min. Passing Marks: **33** |
| PART B: Content of the Course | | | | |
| No. of Lectures (in hours per week): **2 Hrs. per week** | | | | |
| Total No. of Lectures: **60 Hrs.** | | | | |

| Module | Topics | No. of Lectures |
|---|---|---|
| I | **Fundamentals of Digital Electronics**: Data Types, Complements, Fixed-Point Representation, Floating-Point Representation, Binary and other Codes, Error Detection Codes.<br>**Logic Gates**, Boolean Algebra, Map Simplification, Combinational Circuits, Sequential Circuits, simple combinational circuit design problems.<br>**Circuits**- Adder- Subtractor, Multiplexer, Demultiplexer, Decoders, Encoders Flip - Flops, Registers, Counters. | 10 |

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| II | **Basic Computer Organization**: Instruction codes, Computer Registers, Computer Instructions, Timing & Control, Instruction Cycles, Memory Reference Instruction, Input - Output & Interrupts, Complete Computer Description & Design of Basic Computer. | 10 |
|---|---|---|
| III | **Instructions** - Instruction formats, Addressing modes, Instruction codes, Machine language, Assembly language. <br> **Register Transfer and Micro operations** - Register Transfer Language, Register Transfer, Bus & Memory Transfer, Arithmetic Micro-operations, Logic Micro-operations, Shift Micro-operations. | 10 |
| IV | **Processor and Control Unit** - Hardwired vs. Micro programmed Control Unit, General Register Organization, Stack Organization, Instruction Format, Data Transfer & Manipulation, Program Control, Introductory concept of RISC, CISC, advantages and disadvantages of both. <br> **Pipelining** – concept of pipelining, introduction to Pipelined data path and control – Handling Data hazards & Control hazards. | 10 |
| V | **Memory and I/O Systems** - Peripheral Devices, I/O Interface, **Data Transfer Schemes** - Program Control, Interrupt, DMA Transfer. I/O Processor. <br> **Memory Hierarchy**, Processor vs. Memory Speed, High-Speed Memories, Main memory, Auxiliary memory, Cache Memory, Associative Memory, Interleaving, Virtual Memory, Memory Management. | 10 |
| VI | **Parallelism** – meaning, types of parallelism, introduction to Instruction-level-parallelism, Parallel processing challenges, Applications. <br> **Flynn's classification** – Introduction to SISD, SIMD, MISD, MIMD <br> **Hardware multithreading** – Introduction, types, advantages and applications. <br> **Multicore processors** – Introduction, advantages, difference from multiprocessor. | 8 |
| VII | **Indian contribution to the field** – Contributions of reputed scientists of Indian origin - like - Dr. Vinod Dham – Father of Intel Pentium Processor, Dr. Ajay Bhat – Co-Inventor of USB Technology, Dr. Vinod Khosla- co-founder of Sun Microsystems, Dr. Vijay P Bhatkar - architect of India's national initiative in supercomputing, and many others. <br> **Parallel Computing projects of India** – PARAM, ANUPAM, FLOSOLVER, CHIPPS etc. Other relevant contributors and contributions. | 2 |

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**Keywords/Tags:** Digital Electronics, Logic Gates, Circuits, Instruction formats, Addressing Modes, Parallelism, Pipelining, Memory Hierarchy, Multicore, Multithreading, SISD, SIMD, MISD, MIMD, PARAM, ANUPAM, FLOSOLVER, CHIPPS

| PART C: Learning Resources |
|---|
| **Textbooks, Reference Books, Other Resources** |

**Suggested Readings:**

- M.Morris Mano, "Computer System Architecture", PHI.
- Heuring Jordan , "Computer System Design & Architecture" (A.W.L.)
- William Stalling, "Computer Organization & Architecture", Pearson Education Asia.
- V. Carl Hamacher , "Computer Organization", TMH
- Tannenbaum, "Structured Computer Organization", PHI .

**Suggestive digital platform web links :**

https://www.youtube.com/watch?v=4TzMyXmzL8M
https://nptel.ac.in/courses/106/106/106106166/
https://nptel.ac.in/courses/106/106/106106134/

**Suggested  equivalent online courses**

https://nptel.ac.in/courses/106/105/106105163/

| PART D:  Assessment and Evaluation |
|---|

| Internal Assessment : Continuous Comprehensive Evaluation (CCE) : **25 Marks** Shall be based on allotted assignments and Class Tests. The marks shall be as follows: | | External Assessment: University Exam (UE) : **75 Marks** Time : **02.00 Hours** | |
|---|---|---|---|
| Assessment and presentation of assignment | 10 Marks | Section (A) : Three Very Short Questions (50 Words Each ) OR Nine MCQ Questions | 03 x 03 = 09 Marks **OR** 09 x 01 = 09 Marks |
| Class Test I ( **Objective Questions**) | 5 Marks | | |
| Class Test II (**Descriptive Questions**) | 5 Marks | Section  (B) : Four Short Questions (200 Words Each) | 04 x 09 = 36 Marks |
| Class Test III ( **Based on solving circuit design problems**) | 5 Marks | Section (C): Two Long Questions (500 Words Each) | 02 x 15 = 30 Marks |
| Total | **25 Marks** | Total | **75 Marks** |

**Any remarks/suggestions: Learnings in the course should be emphasised more on practical aspects and real world problems and their solutions.**

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| PART A:  Introduction | | | |
|---|---|---|---|
| Program: **Certificate** | Class: **B.Sc.** | Year: **I Year** | Session: **2021-22** |
| Subject: **Computer Science** | | | |

| | | | |
|---|---|---|---|
| 1. | Course Code | S1-COSC1P | |
| 2. | Course Title | **Computer Architecture Lab** **( Paper 1 )** | |
| 3. | Course Type (Core Course/Elective/Generic Elective/ Vocational | **Core Course** | |
| 4. | Pre-Requisite (if any) | To study this course, a student must have had the subject Physics/Maths in 12th class. | |
| 5. | Course Learning Outcomes(CLO) | **On completion of this course, learners will be able to:**<br>1. Realization of the basic logic and universal gates.<br>2. Verify the behavior of logic gates using truth tables.<br>3. Implement Binary-to -Gray, Gray-to -Binary code conversions<br>4. Design half and full adder circuit using basic gates.<br>5. Design and construct flip flops and verify the excitation tables. | |
| 6. | Credit Value | **Practical - 2 Credits** | |
| 7. | Total Marks | Max. Marks : **25+75** | Min. Passing Marks: **33** |

| PART B:  Content of the Course | |
|---|---|
| No. of Lab. Practicals (in hours per week): **2 Hrs. per week** | |
| Total No. of Labs: 30 Hrs | |

| | Suggestive list of Practicals | No. of Labs. |
|---|---|---|
| | 1. To study basic gates (AND, OR, NOT) and verify their truth tables.<br>2. To convert a given binary number to Gray code using IC 7486.<br>3. To study and verify NAND as Universal gate using IC 7400.<br>4. To study half adder using basic gates and verify its truth table.<br>5. To study Full Adder using basic gates and verify its truth table.<br>6. To realize basic gates (AND, OR, NOT) from Universal gates (NAND and NOR).<br>7. To verify truth table of 4-bit adder using IC 7483.<br>8. To design and construct RS flip Flop using gates and verify the truth table.<br>9. To design and construct JK flip Flop using gates and verify the truth table.<br>10. To verify DeMorgan's Theorem. | |

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**Keywords/Tags:** Digital Electronics, Logic Gates, AND, OR, NOT, IC 7486, IC 7400, NAND, NOR, IC 7483, Circuits, Flip Flop, DeMorgan's Theorem

| PART C: Learning Resources |
|---|
| **Textbooks, Reference Books, Other Resources** |

**Suggested Readings:**

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https://nptel.ac.in/courses/106/106/106106134/

**Suggested equivalent online courses**

https://nptel.ac.in/courses/106/105/106105163/

| PART D: Assessment and Evaluation |
|---|

| Internal Assessment : Continuous Comprehensive Evaluation (CCE) : **25 Marks** | | External Assessment: University Exam (UE) : **75 Marks** Time : **02.00 Hours** | |
|---|---|---|---|
| **Internal Assessment** | **Marks** | **External Assessment** | **Marks** |
| Hands-on Lab Practice | 5 Marks | Practical record file | 10 Marks |
| Lab Test from practical list & internal viva | 12 Marks | Viva voce on practical | 15 Marks |
| Assignments (Charts/ Model/ Seminar / Rural Service/ Technology Dissemination/ Report of Excursion/ Lab Visits/ Survey / Industrial visit) | 8 Marks | Table works/ Experiments | 50 Marks |
| **Total** | **25 Marks** | **Total** | **75 Marks** |

**Any remarks/suggestions: Learnings in the course should be emphasised more on real world problems and their solutions.**

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